REMARKS

Claims 1-24 are pending.

Claims 3-11 and 15-23 are objected to.

Claims 1, 2, 12-14 and 24 are rejected.

Applicant thanks the Examiner for discussing the present Office Action, and in particular, the rejections under 35 U.S.C. §102, with Applicant's attorney, on May 6, 2005.

I. SPECIFICATION

The Examiner has objected to the Specification for including the term "generation" instead of "generator" on page 6, line 19 of the Specification. Paper No. 5, page 2. Applicant has amended the Specification accordingly as indicated above.

II. REJECTIONS UNDER 35 U.S.C. §102(b)

The Examiner has rejected claims 1-2 under 35 U.S.C. §102(b) as being anticipated by Buckner et al. (U.S. Patent No. 5,509,037) (hereinafter "Buckner").

As stated above, claim 1 is cancelled and therefore the rejection to claim 1 is moot.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131. Applicant respectfully asserts that Buckner does not disclose "wherein each particular phase of said clock to be asserted to sample said serial data during said period of said serial data corresponds to a particular retiming state" as recited in claim 2. The Examiner in connection with rejecting this claim limitation states:

> [T]he data generated by the data timer 50 corresponds to a particular retiming state, which may be generated, for example, by the CMOS

transmission gates 120-128. See column 5, lines 4-8. Paper No. 5, page 4.

Applicant respectfully traverses. Buckner instead discloses that the outputs from exclusive-NOR gates 110-118 are then provided to complementary MOS (CMOS) transmission gates 120-128, respectively, which are controlled by clock phases Θ_3, Θ_4, Θ_5, Θ_5, and Θ_1, respectively, for Θ_1, Θ_2, Θ_3, Θ_4, and Θ_5 data. Column 5, lines 4-8. There is no language in the cited passage that discloses that transmission gates 120-128 generate particular retiming states. Further, transmission gates 120-128 are not located within data retimer circuit 50 as asserted by the Examiner. Instead, transmission gates 120-128 are located within data transition decoder 44. See Figure 6a. Thus, Buckner does not disclose all of the limitations of claim 2, and thus Buckner does not anticipate claim 2. M.P.E.P. §2131.

III. REJECTIONS UNDER 35 U.S.C. §103(a)

The Examiner has rejected claims 13 and 14 under 35 U.S.C. §103(a) as being unpatentable over Buckner in view of Ducaroir et al. (U.S. Patent No. 6,331,999) (hereinafter "Ducaroir").

A. Claims 13 and 14 are patentable over Buckner in view of Ducaroir

1. The Examiner has not provided any objective evidence or source of motivation for combining Buckner with Ducaroir.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614,

1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Buckner does not teach a transmission medium, a transmitter coupled to the transmission medium where the transmitter is configured to transmit data in a serial form and a receiver coupled to the transmission medium where the receiver receives serial data from the transmission medium transmitted by the transmitter, as recited in claim 13. Paper No. 5, page 5. The Examiner's motivation for modifying Buckner with Ducaroir to include the above-cited claim limitations is "in order to recover a transmitted clock by a receiver as taught by Ducaroir." Paper No. 5, page 6. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness. The Examiner has failed to provide an objective source for his motivation. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 13-14. *Id.*

Further, the Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Buckner) in front of him would modify Buckner to have a transmission medium, a transmitter coupled to the transmission medium where the transmitter is configured to transmit data in a serial form and a receiver coupled to the transmission medium where the receiver receives serial data from the transmission medium transmitted by the transmitter. Buckner teaches a data phase alignment circuit that aligns incoming plesiochronous data with a known clock phase. Abstract. Simply stating "to recover a transmitted clock by a receiver" does not provide any objective reason as to why one of ordinary skill in the art would modify Buckner, which teaches aligning incoming plesiochronous data with a known clock signal, to have a transmission medium, a transmitter coupled to the transmission

medium where the transmitter is configured to transmit data in a serial form and a receiver coupled to the transmission medium where the receiver receives serial data from the transmission medium transmitted by the transmitter.

2. The Examiner has not presented a reasonable expectation of success when combining Buckner with Ducaroir.

The Examiner must present a reasonable expectation of success in combining Buckner with Ducaroir in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

Buckner teaches that in the telecommunications field, telephony, digital, and video data are transmitted and switched by telephone networks at fast data rates. Column 1, lines 30-32. Buckner further teaches that these data may be in any data format, such as DS1, DS3, T1, STS-1, and SONET. Column 1, lines 32-33. In order to properly switch, transmit or perform other data transformation processes, the plesiochronous data must be captured and transformed to one that is synchronous and phase-aligned with respect to a selected clock signal. Column 1, lines 33-37. Buckner further teaches that a need has been identified for a circuitry or method to capture and realign plesiochronous data. Column 1, lines 57-58.

Ducaroir, on the other hand, teaches testing of serial data communication circuits. Column 1, lines 9-11.

The Examiner has not presented any evidence that there would be a reasonable expectation of success in modifying Buckner, which teaches capturing and realigning plesiochronous data that has been transmitted and switched by telephone networks, with Ducaroir, which teaches testing of serial data communication circuits. The Examiner must provide objective evidence as to how Buckner, which teaches capturing and realigning plesiochronous data transmitted by telephone networks, would be combined with Ducaroir, which teaches testing of serial data

communication circuits. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Buckner with Ducaroir. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 13-14. M.P.E.P. §2143.02.

3. Buckner and Ducaroir, taken singly or in combination, do not teach or suggest the following claim limitations.

Applicant respectfully asserts that Buckner and Ducaroir, taken singly or in combination, do not teach or suggest "wherein each particular phase of said clock to be asserted to sample said serial data during said period of said serial data corresponds to a particular retiming state" as recited in claim 14. The Examiner rejects claim 14 under the same rationale as rejecting claim 2. Paper No. 5, page 5. Applicant respectfully traverses the rejection under the same rationale as provided in traversing the rejection of claim 2. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 14, since the Examiner is relying upon an incorrect, factual predicate in support of the rejections. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

The Examiner has further rejected claims 12 and 24 under 35 U.S.C. §103(a) as being unpatentable over Buckner in view of Lee et al. (U.S. Patent No. 6,266,799) (hereinafter "Lee").

B. Claims 12 and 14 are patentable over Buckner in view of Lee

1. The Examiner has not provided any objective evidence or source of motivation for combining Buckner with Lee.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to

make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Buckner does not teach an oscillator operating at a frequency lower than a data rate of the serial data, as recited in claims 12 and 24. Paper No. 5, page 6. The Examiner's motivation for modifying Buckner with Lee to include the above-cited claim limitations is "for the purpose of saving power or synchronize data and clock before the data is transferred to other circuitry." Paper No. 5, page 7. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness. The Examiner has failed to provide an objective source for his motivation. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 12 and 24. *Id.*

Further, the Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Buckner) in front of him would modify Buckner to have an oscillator (element 43) operate at a frequency lower than the data rate of the serial data. Buckner teaches a data phase alignment circuit that aligns incoming plesiochronous data with a known clock phase. Abstract. Simply stating "for the purpose of saving power or synchronize data and clock before the data is transferred to other circuitry" does not provide any objective reason as to why one of ordinary skill in the art would modify Buckner, which teaches aligning incoming plesiochronous data with a known clock signal, to have an oscillator (element 43) operate at a frequency lower than the data rate of the serial data.

2. The Examiner has not presented a reasonable expectation of success when modifying Buckner to have its oscillator operate at a frequency lower than the data rate of the serial data.

The Examiner must present a reasonable expectation of success in modifying Buckner to have its oscillator (element 43) operate at a frequency lower than the data rate of the serial data in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

Buckner teaches a telephony switch that includes a phase-locked loop which generates multiple phases of a clock signal. Column 3, lines 26-28. Buckner further teaches data phase alignment circuitry that receives the phases generated by the phase-locked loop and aligns the serial data with a selected phase of the clock signal. Column 3, lines 34-36. Buckner further teaches that the phase-locked loop includes a phase detector coupled to a voltage-controlled oscillator (element 43). Column 3, lines 47-48. Buckner further teaches that the phase detector compares the input clock signal with a divided down output from the voltage-controlled oscillator (element 43) and generates an error voltage. Column 3, lines 48-50. Buckner further teaches that the error voltage is received by the voltage-controlled oscillator (element 43) and that the voltage-controlled oscillator (element 43) outputs multiple phases of the internal clock. Column 3, lines 50-55.

The Examiner has not presented any evidence that by modifying the voltage-controlled oscillator (element 43), described above, to have its operating frequency lower than the data rate of the serial data, the voltage-controlled oscillator (element 43) would still be able to perform, as described in Buckner, in order to align plesiochronous data to a known clock phase. The Examiner must provide objective evidence that there would be a reasonable expectation of success in modifying the voltage-controlled oscillator (element 43), described above, to have its operating frequency lower than the data rate of the serial data and that the voltage-controlled oscillator (element 43) would still be able to perform, as described in Buckner, in

order to align plesiochronous data to a known clock phase. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in modifying Buckner to have its oscillator (element 43) operate at a frequency lower than the data rate of the serial data. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 12 and 24. M.P.E.P. §2143.02.

3 By combining Buckner with Lee, the principle of operation of Buckner would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactorily for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Applicant submits that by combining Buckner with Lee, the principle of operation in Buckner would change and subsequently render the operation of Buckner to perform its purpose unsatisfactorily.

Buckner teaches a telephony switch that includes a phase-locked loop which generates multiple phases of a clock signal. Column 3, lines 26-28. Buckner further teaches that the phases of the clock signal generated by the phase-locked loop are received by a data phase alignment circuitry configured to align the received data with a selected phase of the clock signal. Column 3, lines 28-36. Buckner further teaches that the aligned data is then provided to a switching matrix which switches and routes the data to the desired outputs of the matrix. Column 3, lines 37-39. Buckner further teaches that there is a need to capture and realign plesiochronous data. Column 1, lines 57-58.

Lee, on the other hand, teaches a multi-phase data/clock recovery unit which receives incoming data and ensures that the clock is synchronized with the incoming data. Column 5, lines 9-12. Lee further teaches that the multi-phase data/clock recover unit receives multiple clock phases from a multi-phase clock generator. Column 5, lines 40-43. Lee further teaches that the multi-phase clock generator provides the phases to a multiplexer within the multi-phase data/clock recovery unit which is controlled by a decoder. Column 5, line 67 – column 6, line 2. Lee further teaches that the multiplexer includes four-phase sampler circuit which receives these phases. Column 6, lines 7-8. Lee further teaches that the four-phase sampler circuit communicates the location of those phases with respect to the incoming data and/data to a transition detect and lead-lag decision circuit. Column 6, lines 8-12. Lee further teaches that the transition detect and lead-lag decision circuit ascertains whether the clock is either leading or lagging the data based upon the selected phases. Column 6, lines 12-15. Lee further teaches that if it is determined that the clock is lagging the data, then the transition detect and lead-lag decision circuit will trigger an UP command that is transferred to an UP-DOWN counter. Column 6, lines 16-19. Lee further teaches that if it is determined that the transition detect and lead-lag decision circuit ascertains that the clock leads the data transition, then a DOWN command will be passed to the UP-DOWN counter. Column 6, lines 19-22. Lee further teaches that it is the UP-DOWN counter that will shift the clock ahead if the clock is lagging the data transition, or will shift the clock back if the clock leads the data transition. Column 6, lines 23-25.

By combining Buckner with Lee, Buckner would no longer be able to align plesiochronous data with a selected phase of a clock signal. As stated above, Buckner teaches that its purpose is to capture and realign plesiochronous data. However, as stated above, Lee teaches shifting the clock either ahead of behind depending on whether the clock signal is lagging or leading the data transition. Hence, Lee teaches shifting the clock signal instead of aligning the data with a phrase of the clock signal.

By combining Buckner with Lee, Buckner would be modified to shift a clock signal based on whether the clock signal is lagging or leading the data transition instead of aligning the data with a phrase of the clock signal. Thus, by combining Buckner with Lee, the principle of operation in Buckner would change, and subsequently render the operation of Buckner to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 12 and 24 *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984); *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959).

4. Applicant traverses the Examiner's assertion that an oscillator operating at a frequency lower than a data rate of the serial data is well known in the art.

The Examiner asserts that it appears to be well known in the art for the oscillator of Buckner to generate phases of a clock to operate at a frequency lower than the data rate of the serial data inputted to the receiver. Paper No. 5, page 6. Applicant respectfully traverses. There is no language in Buckner that teaches or suggests that the oscillator (element 43) in Buckner operates at a frequency lower than the data rate of the serial data.

The Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Buckner to have its oscillator (element 43) operate at a frequency lower than the data rate of the serial data. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner has not provided any motivation for modifying Buckner to have its oscillator (element 43) operate at a frequency lower than the data rate of the serial data. In order to support a *prima facie* case of obviousness, the Examiner must provide a motivation to modify Buckner to have its oscillator (element 43) operate at a frequency lower than the data rate of the serial data. M.P.E.P. §2143. Since the Examiner has not provided any motivation, the Examiner has not provided a *prima facie* case of obviousness in rejecting claims 12 and 24. *Id.*

5. Buckner and Lee, taken singly or in combination do not teach or suggest the following claim limitations.

Applicant respectfully asserts that Buckner and Lee, taken singly or in combination, do not teach or suggest "wherein said oscillator operates at a frequency lower than a data rate of said serial data" as recited in claim 12 and similarly in claim 24. The Examiner cites column 5, lines 52-58 of Lee as teaching the above-cited claim limitation. Paper No. 5, page 7. Applicant respectfully traverses and asserts that Lee instead teaches a phase-locked loop circuit having a VCO where the VCO produces a clock signal and the timing signal and where the serial data stream is sampled within each data window dependent upon the duty cycle of the timing signal and where the VCO varies the duty cycle of the timing signal according to a received control signal in order to facilitate measurement of the amount of jitter within the serial data stream. Column 5, lines 52-62. There is no language in the cited passage that teaches that the VCO operates at a frequency lower than the data rate of the serial data. Lee simply teaches that the serial data stream is sampled within each data window dependent upon the duty cycle of a timing signal. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 12 and 24, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

IV. ALLOWABLE SUBJECT MATTER

Applicant appreciates the indication of allowability of claims 3-11 and 15-23.

V. CONCLUSION

As a result of the foregoing, it is asserted by Applicant that claims 2-24 in the Application are in condition for allowance, and Applicant respectfully requests an allowance of such claims. Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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